

Genetic Algorithms and their use in the design of Evolvable Hardware.

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Concept of Genetic Algorithms

- w Modeled on Biological Evolution

- w Idea of Optimization in Nature

- w *Nature's method to evolve optimal solutions without the hindrance of preconceived knowledge.*

- Prof. John Koza



Biological Background

- w Survival of the Fittest *-Charles Darwin*
- w The best genes are transferred to the next generation.
- w The Reproduction Process
- w Fitness of an Individual.

A decorative graphic on the left side of the slide, resembling a DNA double helix. It is composed of two intertwined strands, one colored in shades of pink and the other in shades of purple. The strands are connected by horizontal rungs, creating a spiral effect that runs vertically down the left margin.

Development of a GA:

```
Simple_Genetic_Algorithm()  
{  
    Initialize the Population;  
    Calculate Fitness Function;  
  
    While(Fitness Value != Optimal Value)  
    {  
        Selection;  
        Crossover;  
        Mutation;  
        Calculate Fitness Function;  
    }  
}
```



Steps in a Genetic Algorithm:

- w Population
- w Selection
- w Encoding
- w Crossover
- w Mutation
- w Elitism
- w Offspring



Examples:

- w Genetic Algorithm examples in Java
- w The working : A simple applet
- w The mechanics : Minimization of a Function



Evolvable Hardware

- w Autonomous Adaptation
- w On-line Adaptation
- w Un-supervised Learning
- w Characteristics of Problem not known in advance.
- w “Intelligent” Machines



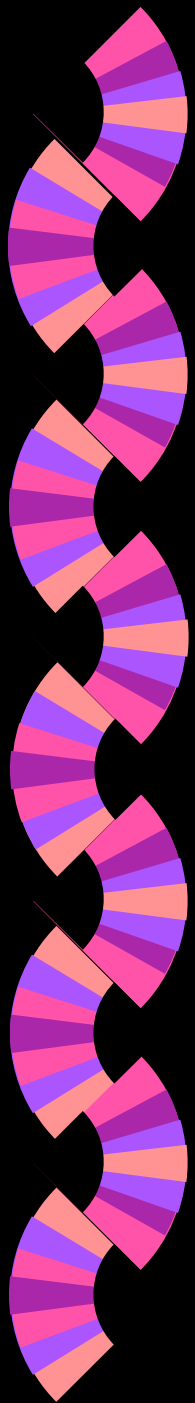
Why GA's for EHW ?

- w Why GA's are an effective solution to developing Evolvable Hardware*
- w Configuration Bits = Chromosomes*
- w Fitness Function = Performance*
- w No knowledge of search-space required*
- w Continuous Reconfiguration*



Why Evolvable Hardware ?

- w The utility and importance of Evolvable Hardware in ...*
- w Data Compression Hardware**
- w Artificial Neural Networks**
- w Ontogenic Neural Networks**



The GRD Chip:

A practical implementation

- w Genetic Reconfiguration of DSP's.
- w In April 1999, by Japanese Scientists.
- w 32-bit RISC Processor @ 100 MHz (NEC V830).
- w Binary Tree Network of 15 16-bit DSP's @ 33 MHz.



Applications of the GRD Chip

- w Dynamic Reconfiguration of DSPs
- w Embedded Systems in practical Industrial Applications.
- w Ontogenic Neural Networks
- w Adaptive Equalization



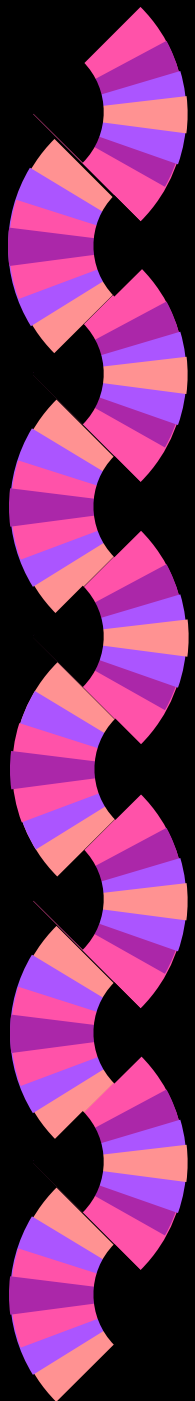
Scope & Limitations:

- w Excellent Solution, but not for all problems
- w Vast Search Space
- w Embryonic Circuits (LC, RC, etc)

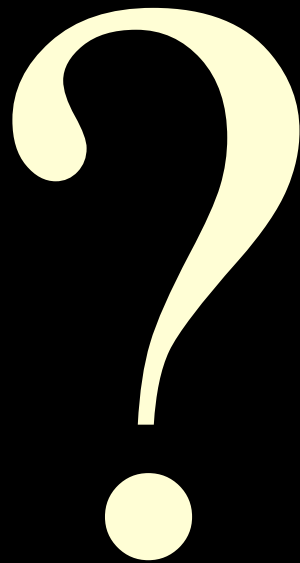


Concluding Remarks:

- w A promising area
- w Although a rich set of methods is available, a lot of options are open to research.
- w Scope for further research & development are immense



Questions ?





Reference:

w This paper is available online at:

<http://www.manastungare.com/articles/>

w *Our sincere thanks to:*
Prof. Sasi Kumar, NCST.